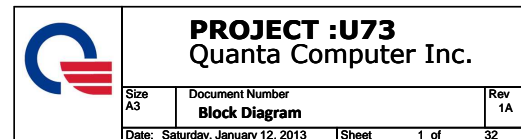
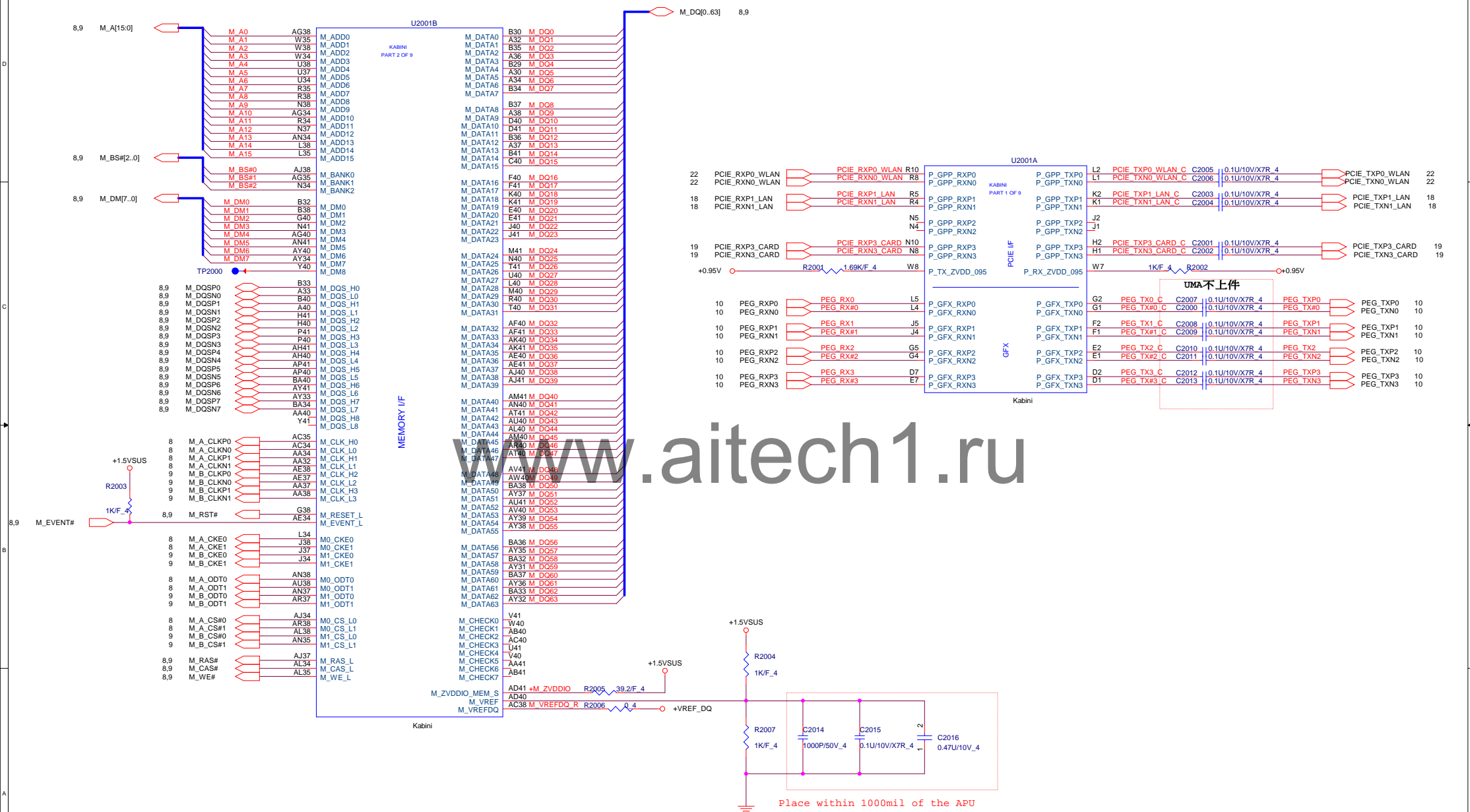
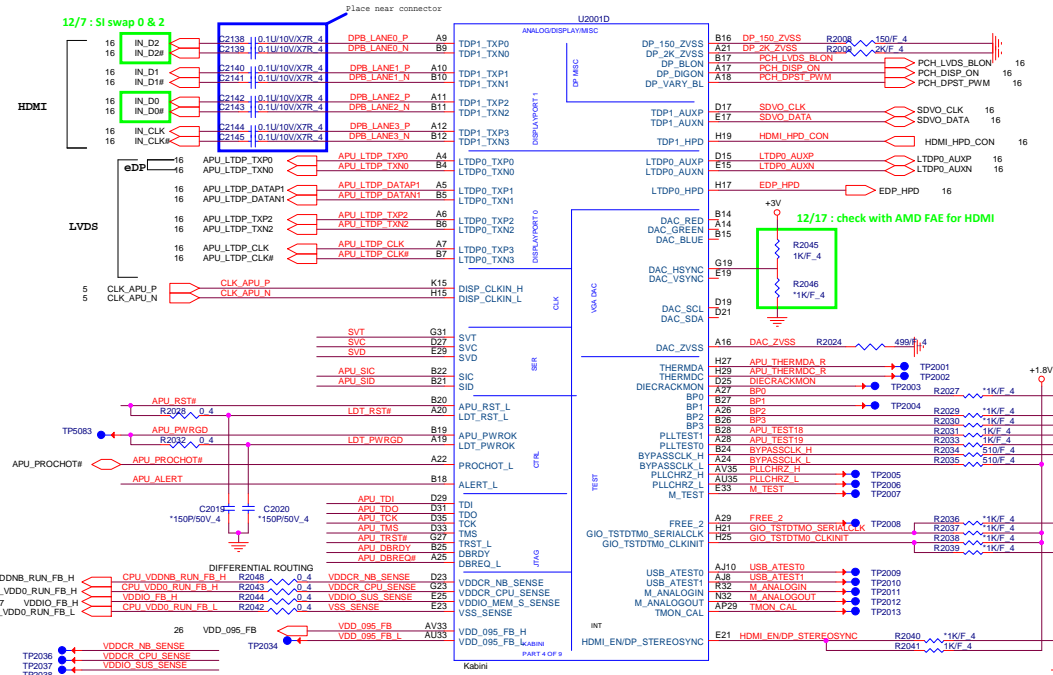
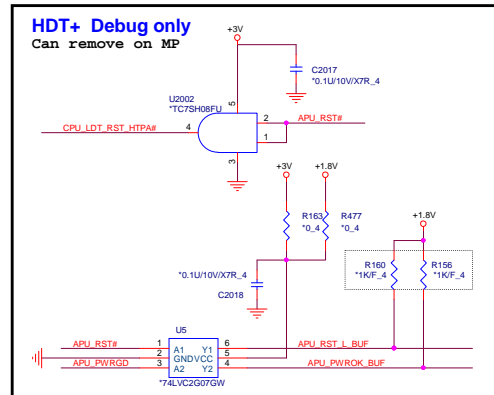
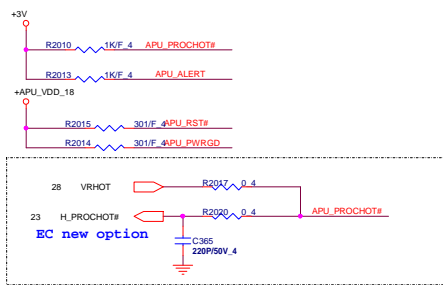


Ultra/Slim⁰¹

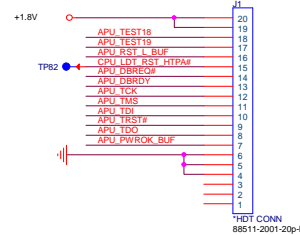
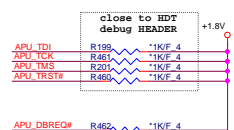




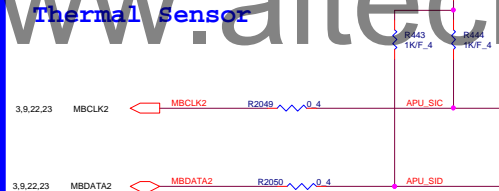
6,8,9,27,30,32 +1.5VSUS
8,9 +VREF_DQ
5,6,26 +0.95V



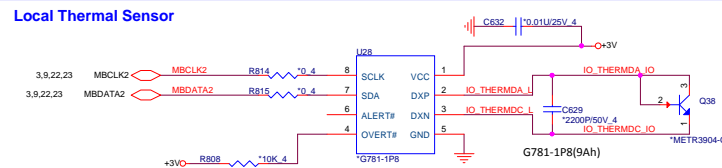
HDT+ Connector for Debug only



Thermal Sensor

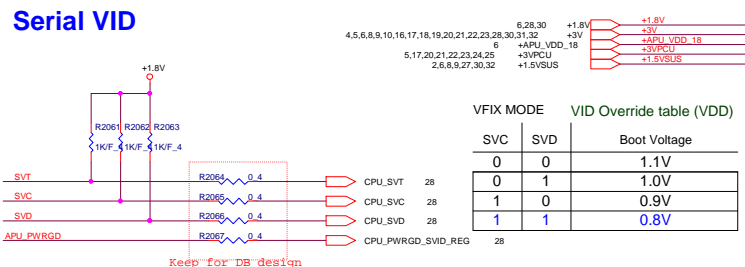


Local Thermal Sensor

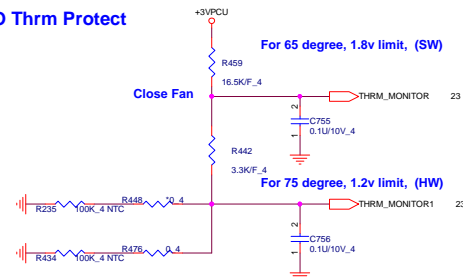


Place under CPU heat pipe

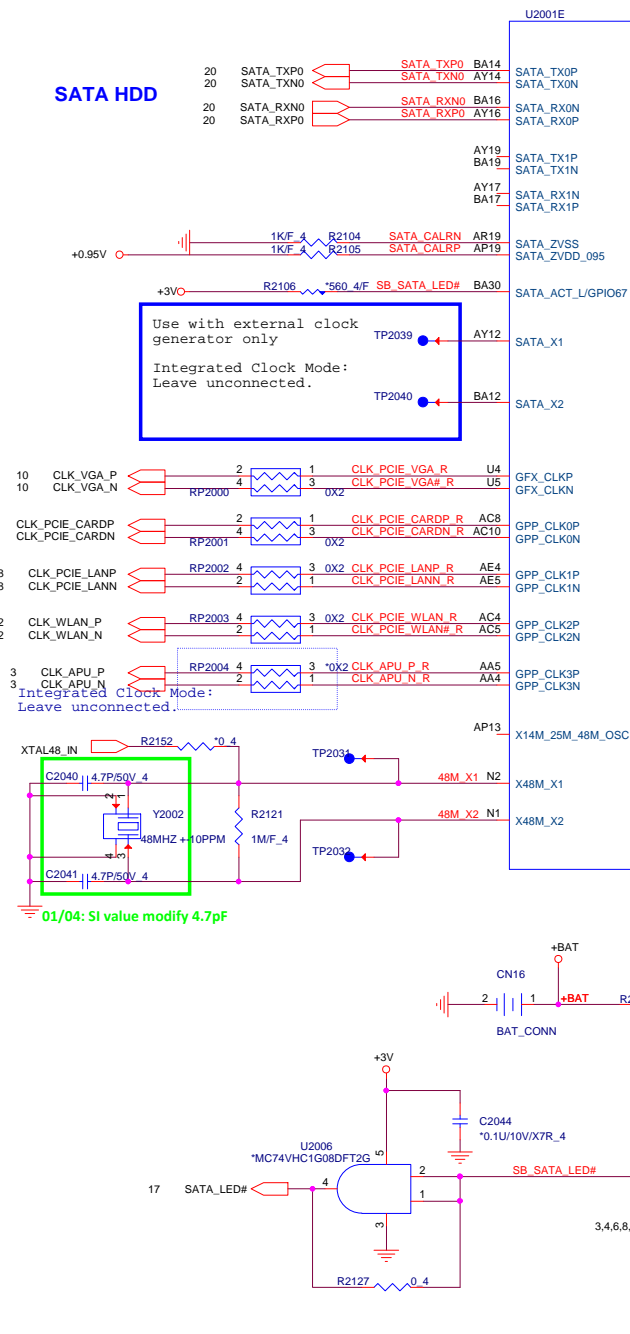
Serial VID



IO Thrm Protect



SATA HDD



BOARD ID SETTING

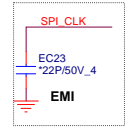
Model	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4
14" UMA	0	0	0	0	0
15" UMA	0	1	0	0	0
14" DIS	1	0	0	0	0
15" DIS	1	1	0	0	0

www.aitech1.ru

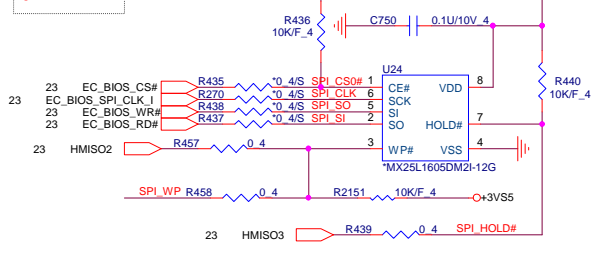
APU SPI ROM

Replace to MX25L6436E


Vender	Size	P/N
AMIC	2M	AKE38ZN0801
WINBOND	2M	AKE38FP0N01
Socket		DFHS08FS023



EMI

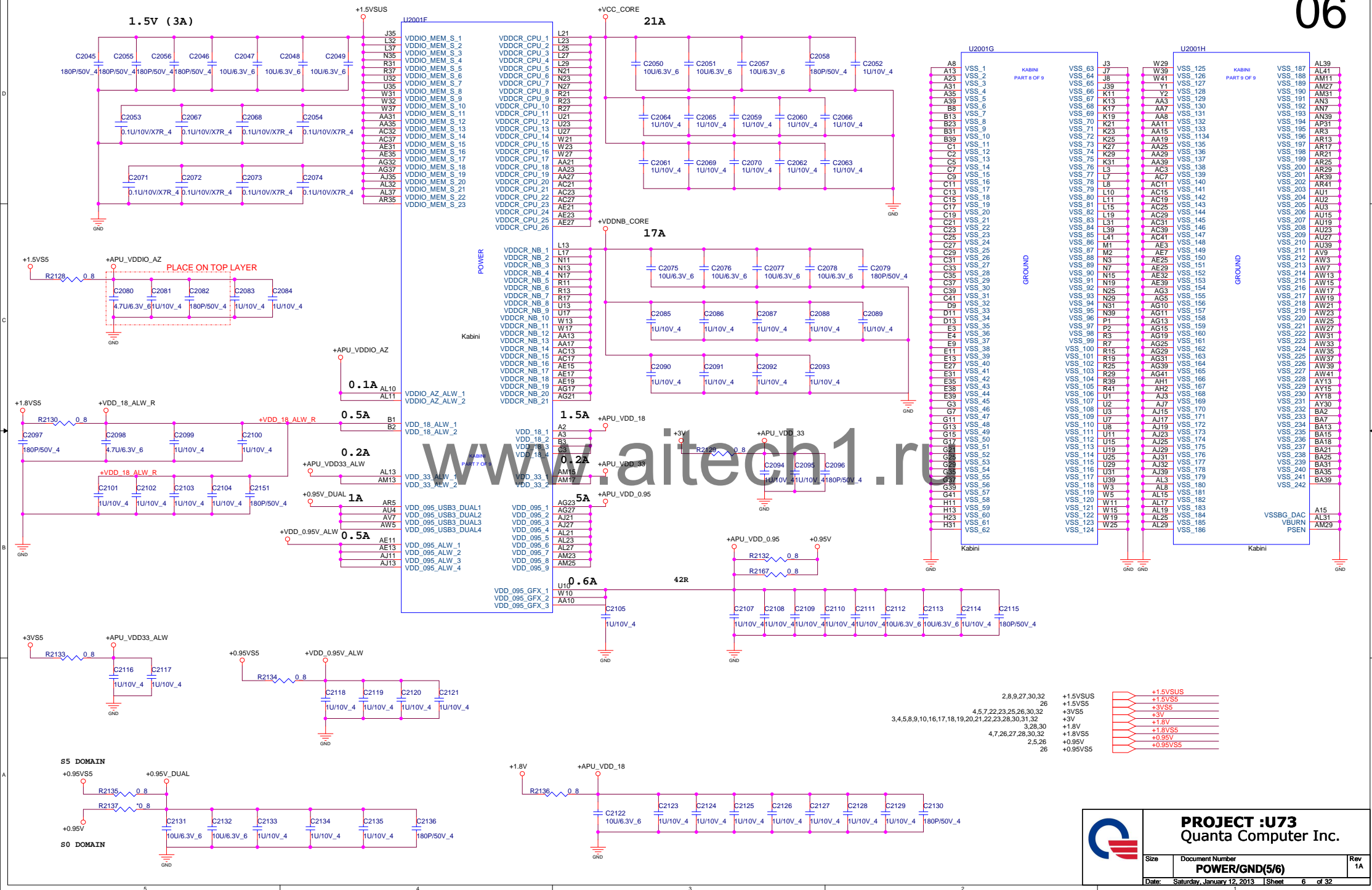


un-mount



PROJECT :U73
Quanta Computer Inc.

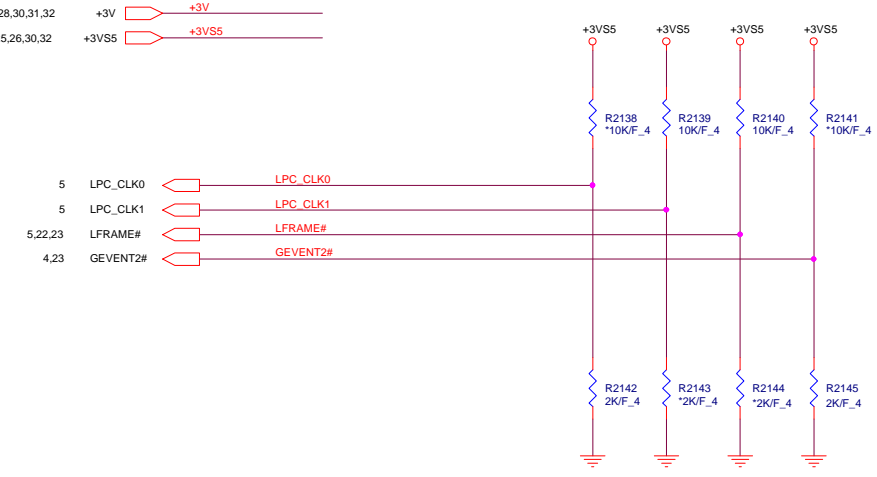
Size	Document Number	Rev
	SATA/CLK (4/6)	1A
Date:	Saturday, January 12, 2013	Sheet 5 of 32



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

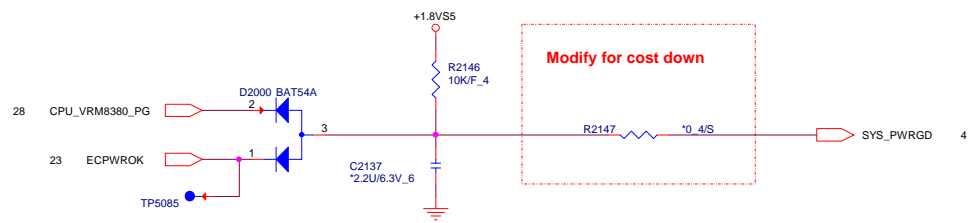
DEBUG STRAPS

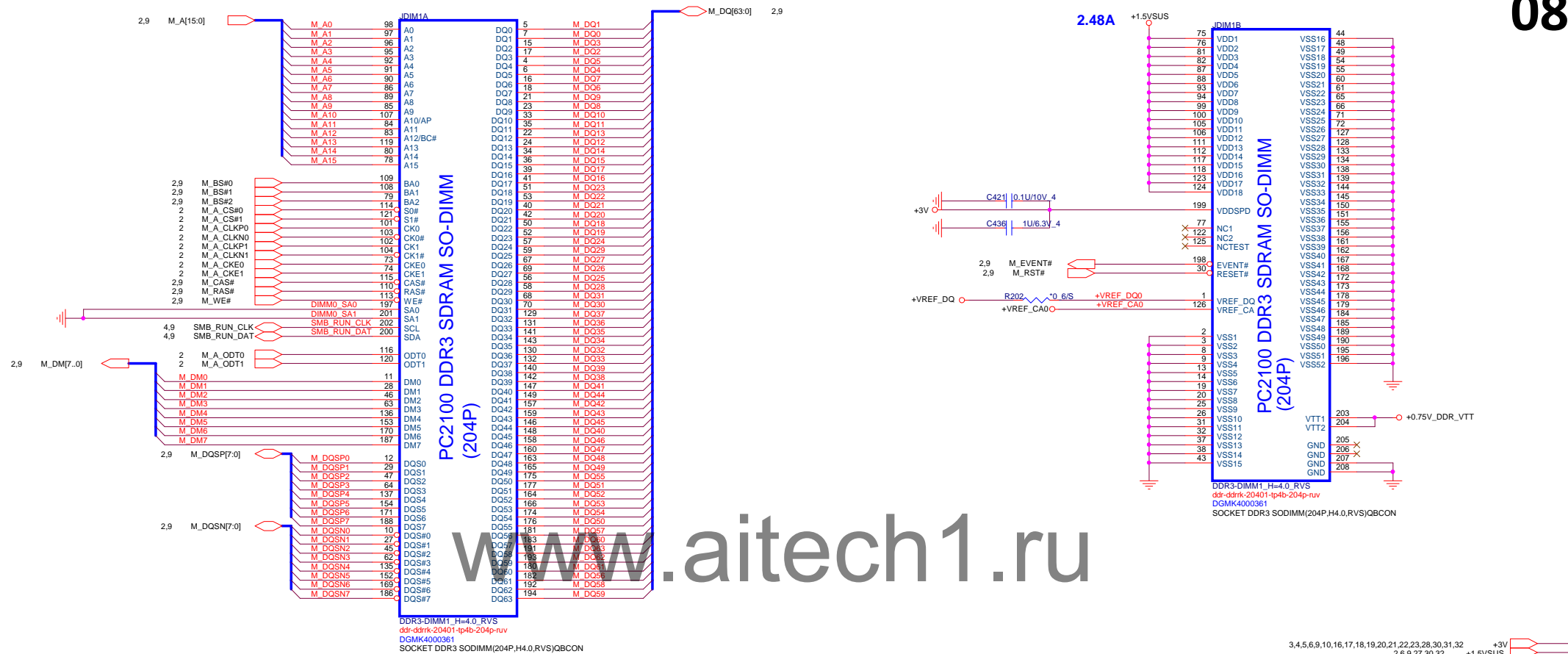


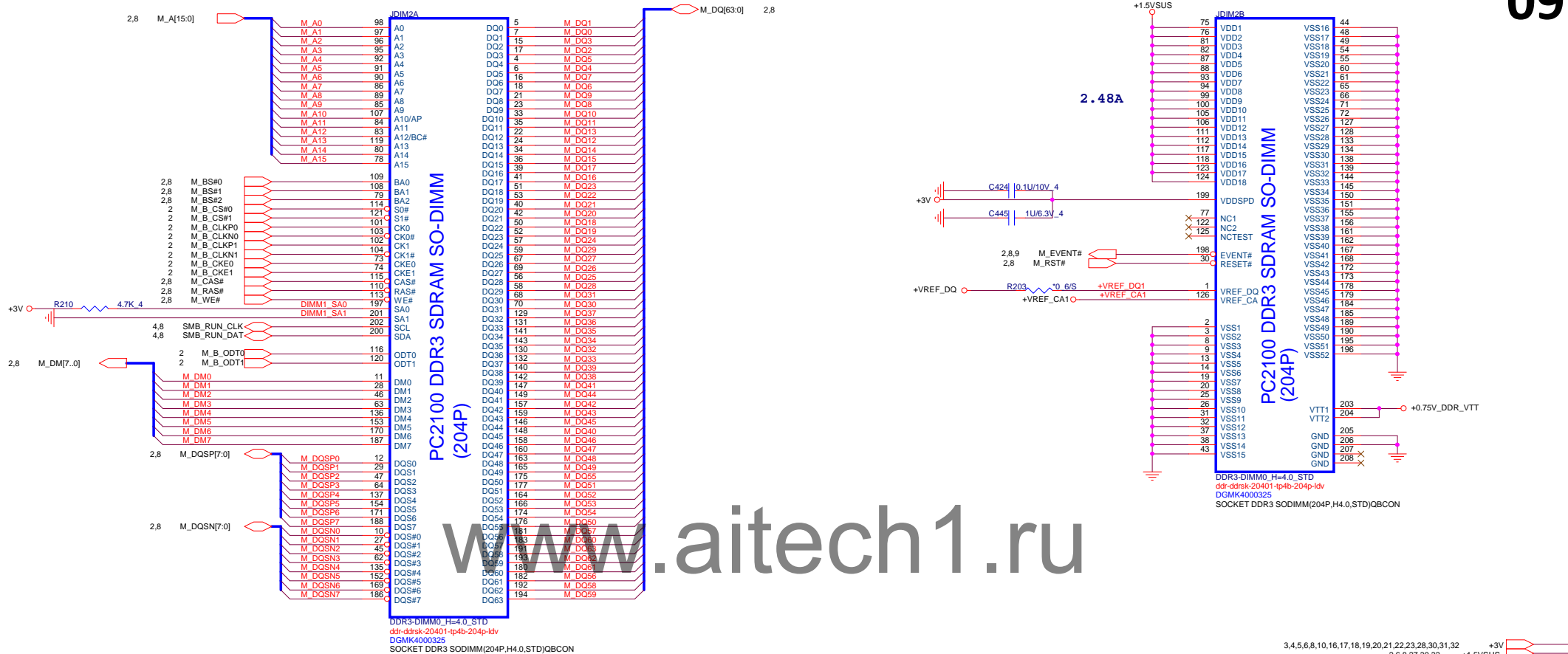
REQUIRED STRAPS

					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED	SPI ROM	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM
					DEFAULT	DEFAULT	DEFAULT	DEFAULT

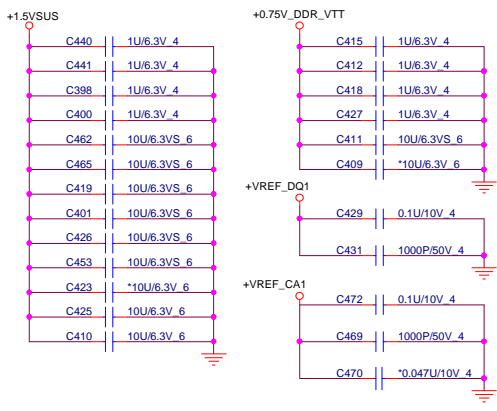
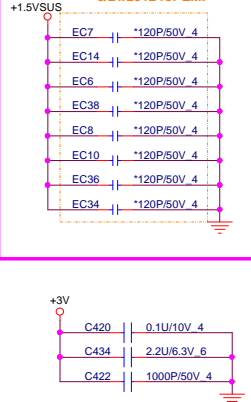
SYS_PWRGD





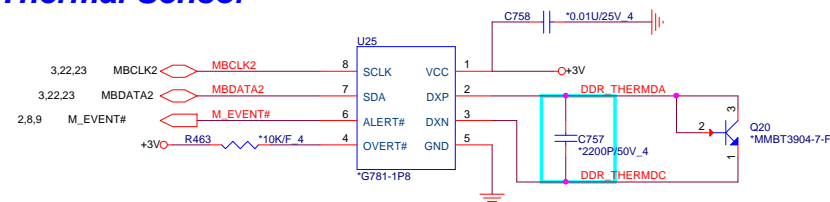


Place these Caps near So-Dimm1.

For EMI RESERVE
6/21/2012 for EMI

Local Thermal Sensor

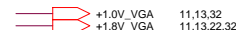
DDR3 Thermal Sensor



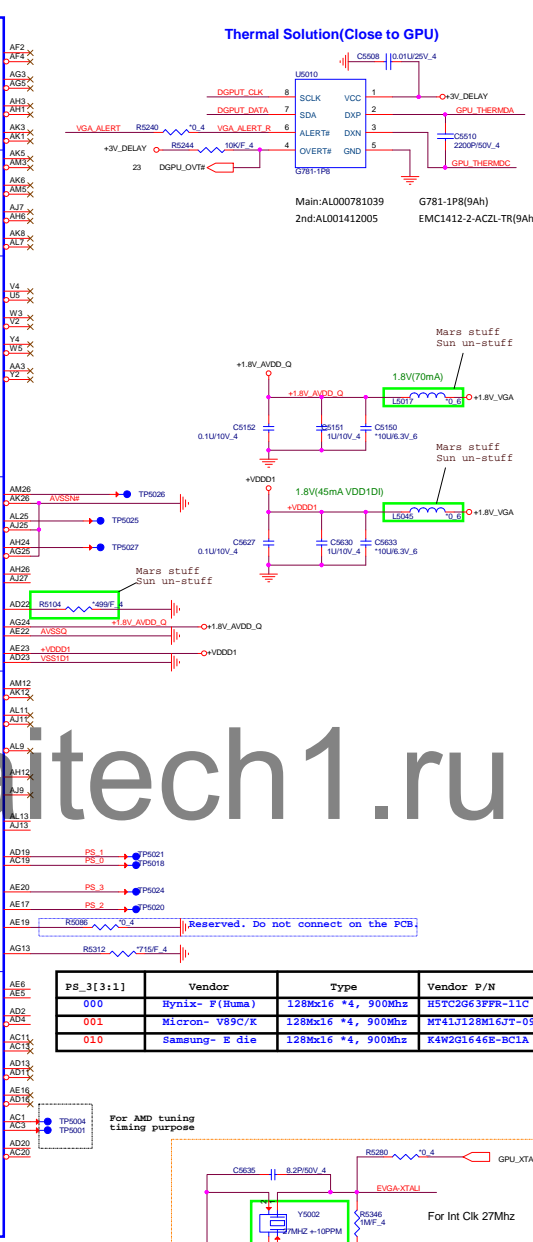
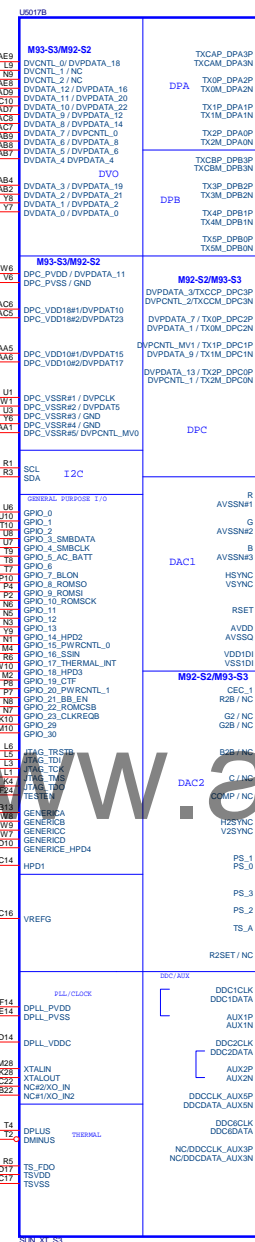
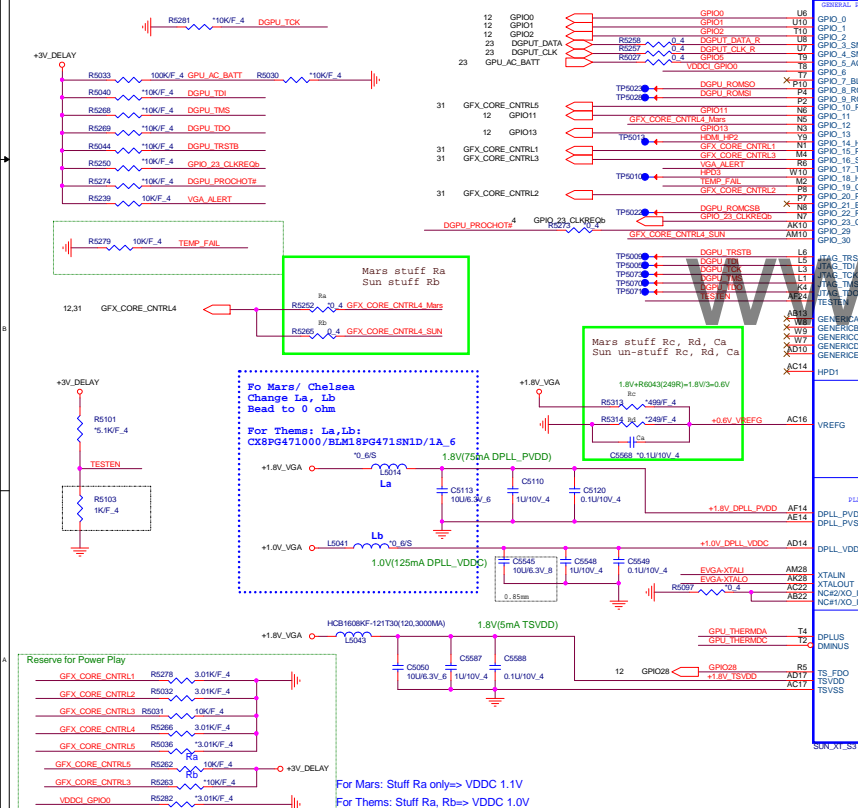
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

PROJECT :U73 Quanta Computer Inc.		
Size Custom	Document Number System Memory 2/2 (9.2H)	Rev 1A
Date: Saturday, January 12, 2013	Sheet 9	of 32



GPIO3	GPIO12	GPIO16	GPIO20	GPIO15	Sun S3
PWRCTRL4	PWRCTRL3	PWRCTRL2	PWRCTRL1	PWRCTRL0	V-CORE
0	0	0	0	0	1.0V
0	0	0	0	1	0.9V
0	0	0	1	0	0.875V
0	0	0	1	1	0.85V
0	0	1	0	0	0.8V
0	0	1	0	1	0.75V



MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_{pu}, R_{pd} and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

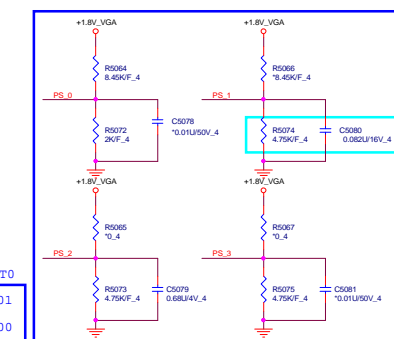
R _{pu} (Ohm)	R _{pd} (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidfg[2:0] define memory aperture size If bios_rom_en = 1, romidfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrsv_erb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disabled: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_cp[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[4]	aud_port_cp[1]			
PS_0[5]	aud_port_cp[0]			

PS_3[3:1]	Vendor	Type	Vendor P/N	R5067	R5075
000	Hynix- F(Ruma)	128Mx16 *4, 900Mhz	H5TC2G63FPR-11C	NC	4.75K
001	Micron- V89C/K	128Mx16 *4, 900Mhz	MT41J128M16JT-093G1K	8.45K	2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4W2G1646E-BC1A	4.53K	2K

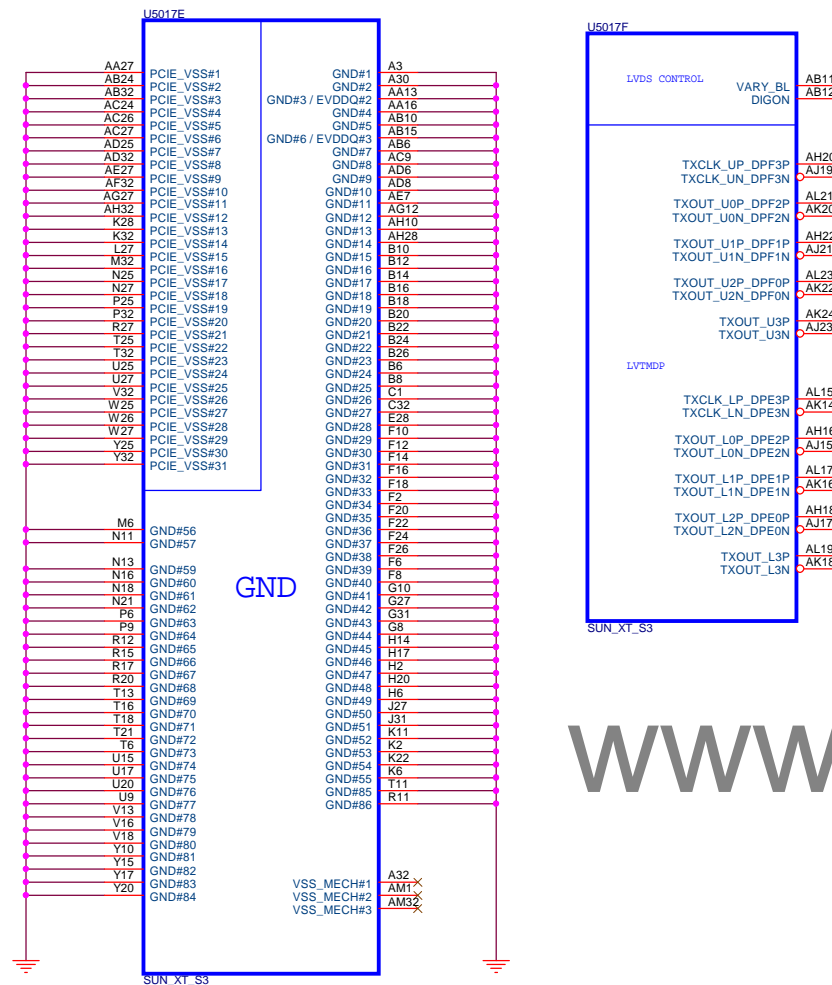
BIT5 => BIT0

PS0	=>	11001
PS1	=>	01000
PS2	=>	00000
PS3	=>	11000



PROJECT :U73
Quanta Computer Inc.

Doc Custom Document Number
Sun S3 Main
Date: Saturday, January 12, 2013 11:00 AM
Sheet 11 of 30



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1= INSTALL 3K RESISTOR
X= DESIGN DEPENDANT
NA= NOT APPLICABLE

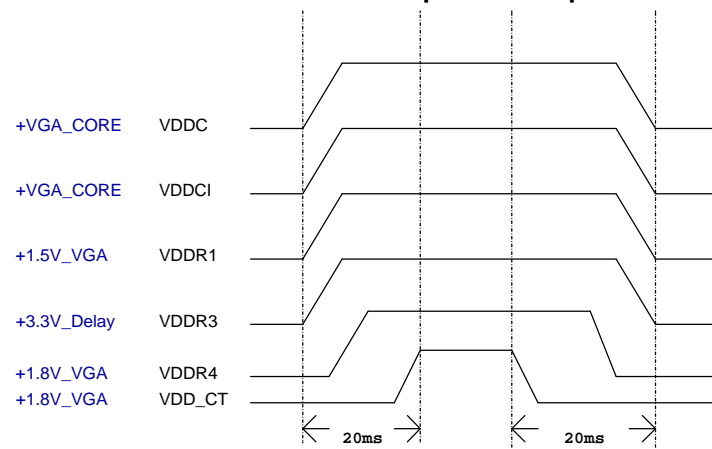
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIOQ[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

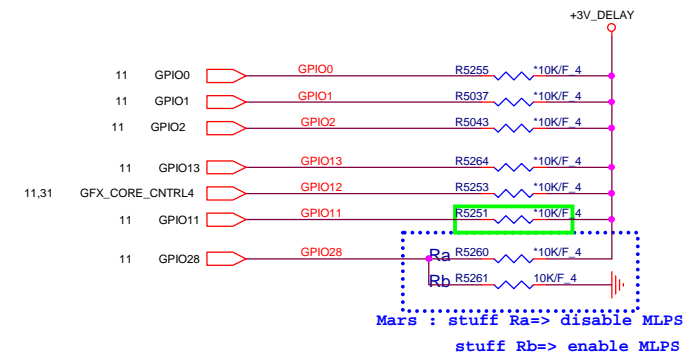
Power Up/Down Sequence



Memory Aperture size(Seymour)

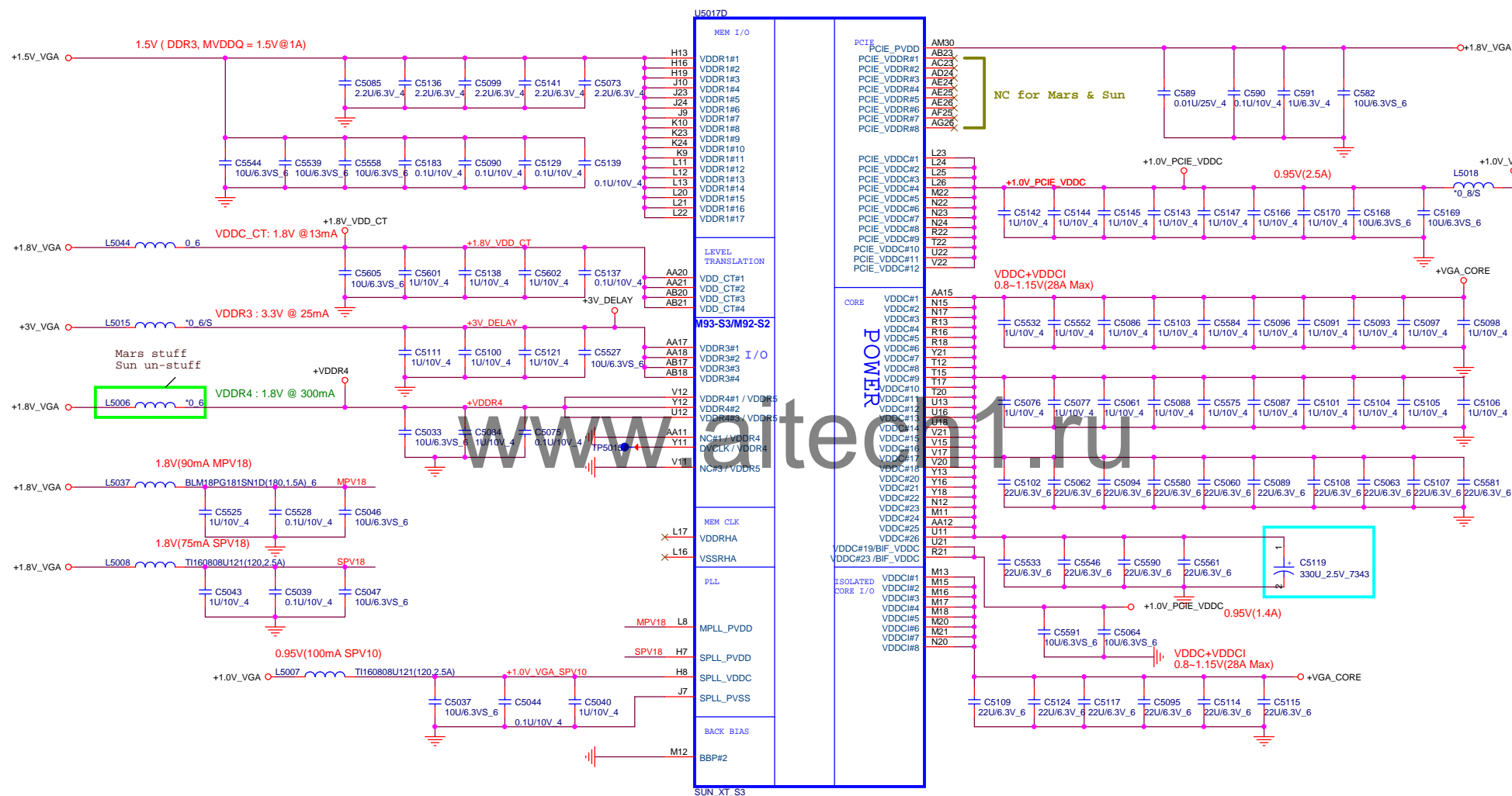
GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

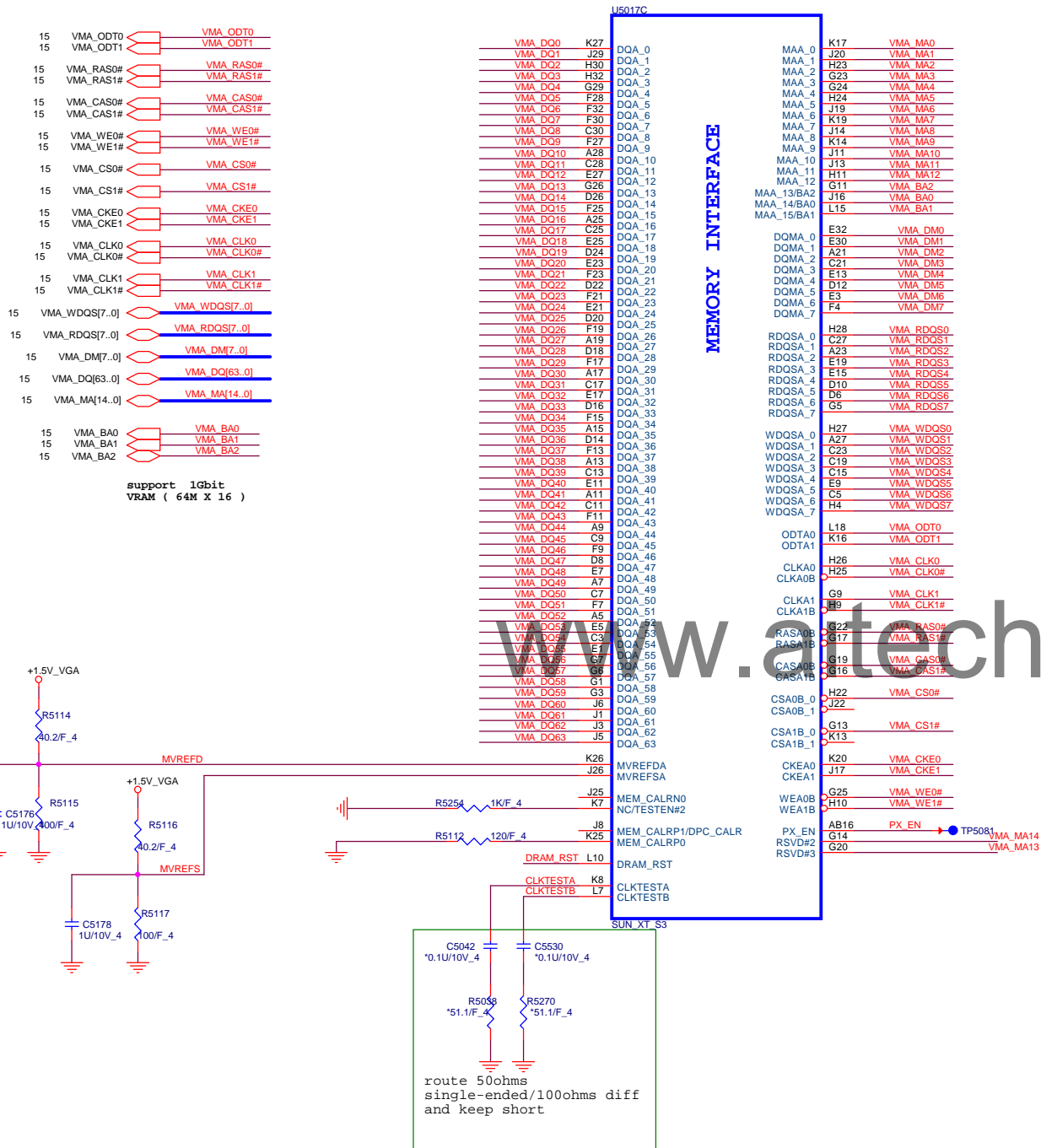
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



PROJECT :U73
Quanta Computer Inc.

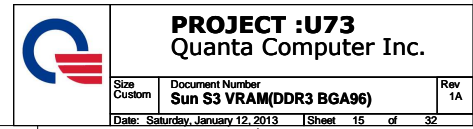
Size Custom	Document Number Sun S3 GND / LVDS/ Straps	Rev 1A
Date: Saturday, January 12, 2013	Sheet 12 of 32	



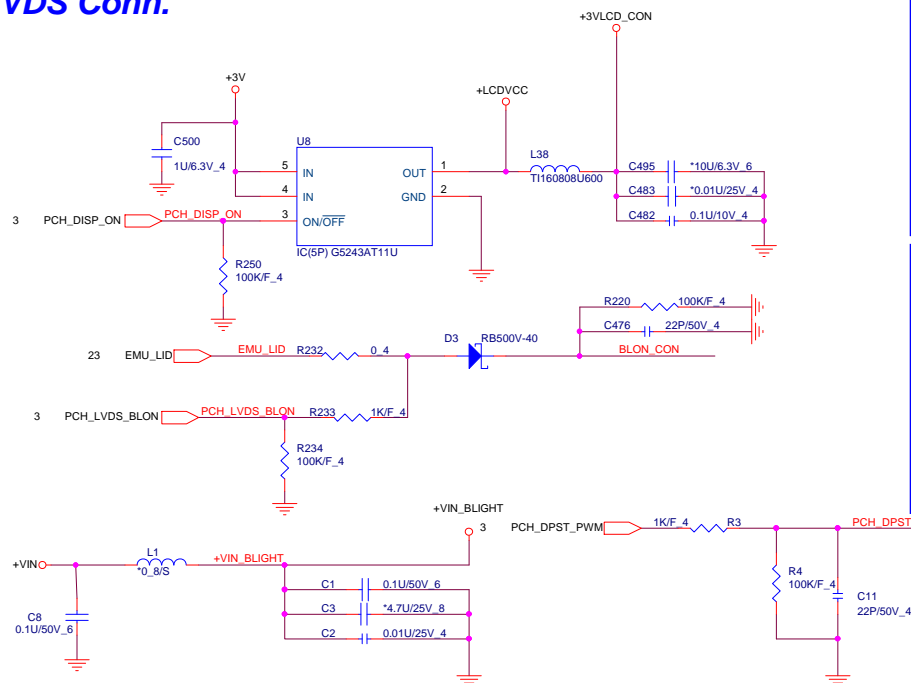


PROJECT :U73
Quanta Computer Inc.

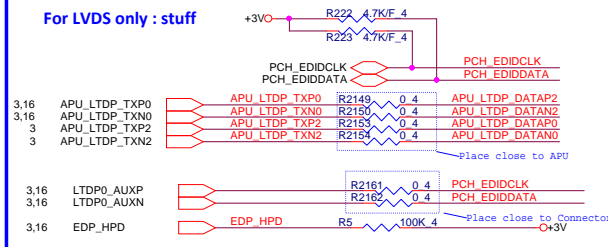
Size	Document Number	Rev
Custom	Sun S3 MEM_Interface	1A
Date: Saturday, January 12, 2013	Sheet 14 of 32	



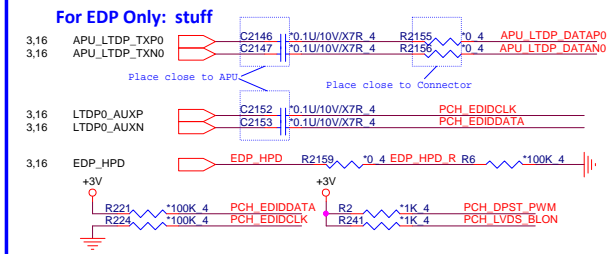
LVDS Conn.



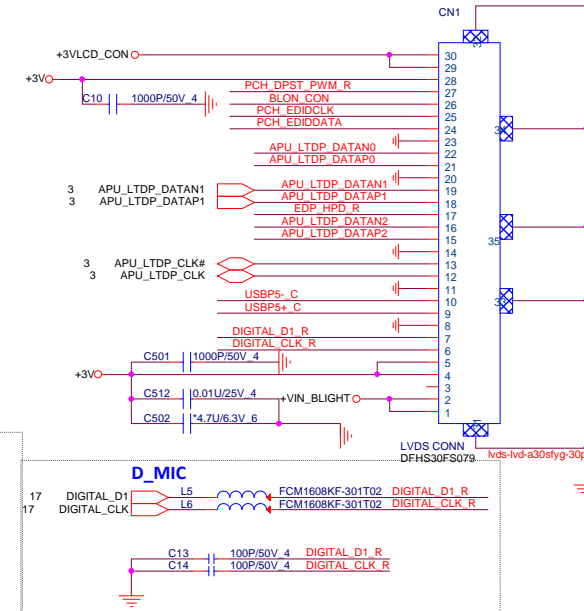
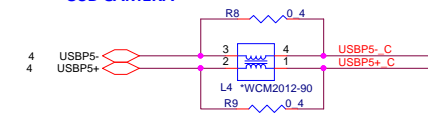
For LVDS only : stuff



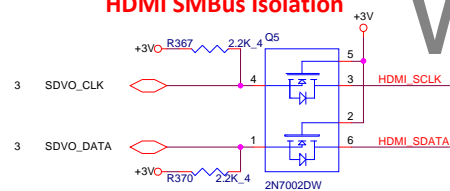
For EDP Only: stuff



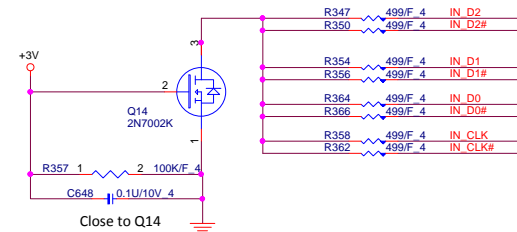
USB CAMERA

**HDMI Conn.**

HDMI SMBus Isolation

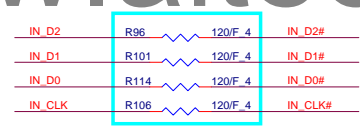


Close to HDMI connector

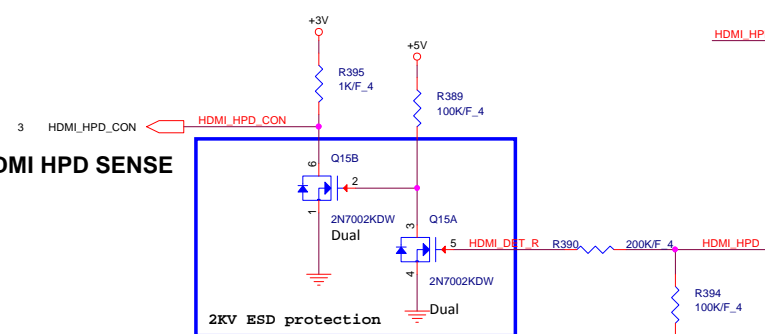


Close to Q14

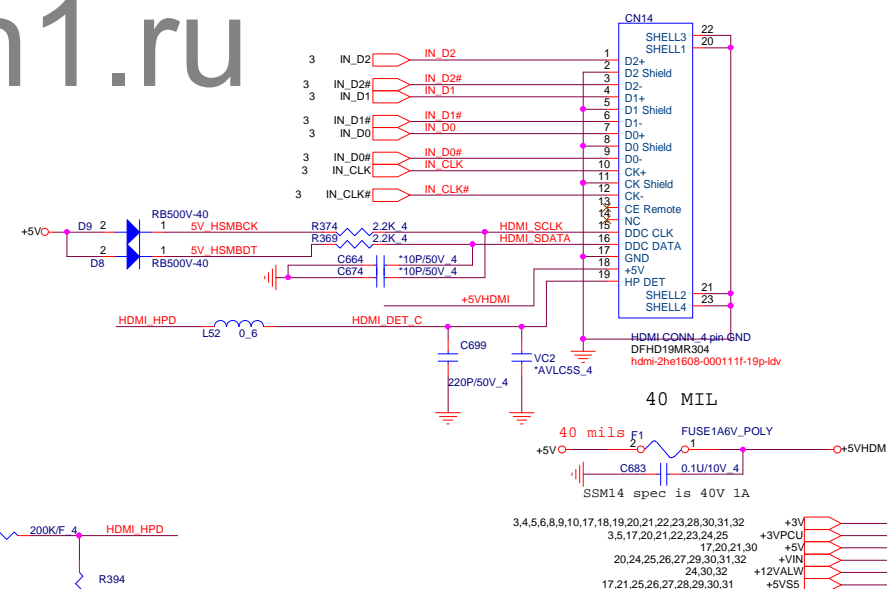
EMI Solution



HDMI HPD SENSE



2KV ESD protection



40 MIL

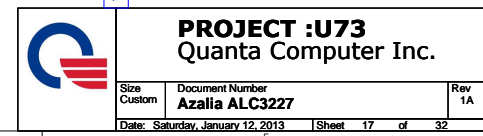
40 mms F1 FUSE1A6V_P
+5V 2 1
C683 0.1U/10V 4
SSM14 spec is 40V 1A

3,4,5,6,8,9,10,17,18,19,20,21,22,23,28,30,31,32	+3V
3,5,17,20,21,22,23,24,25	+3VPCU
17,20,21,30	+5V
20,24,25,26,27,29,30,31,32	+VIN
24,30,32	+12VALW
17,21,25,26,27,28,29,30,31	+5VS5



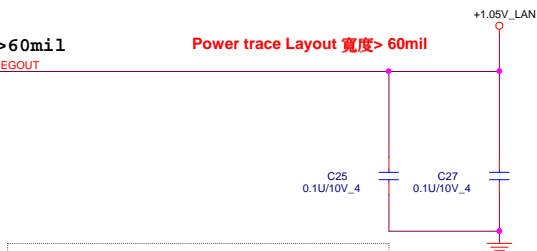
PROJECT :U73
Quanta Computer Inc.

Size Custom	Document Number LCD Connector (LVDS)	Rev 1A
Date: Saturday, January 12, 2013		Sheet 16 of 32

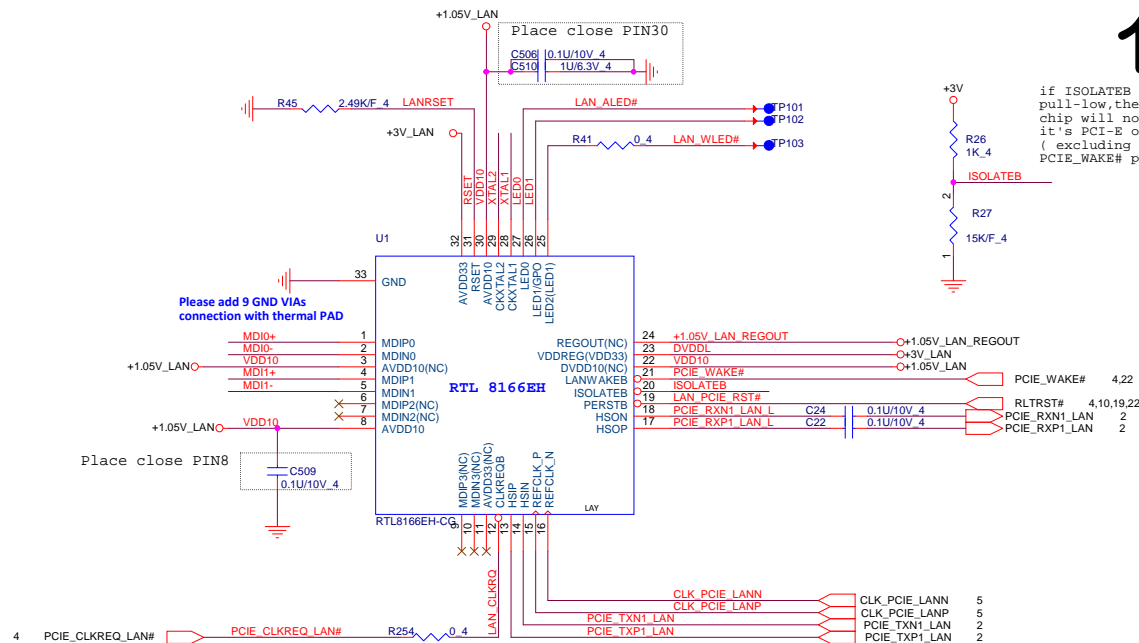
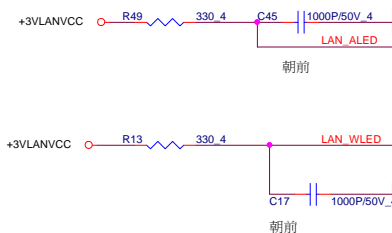
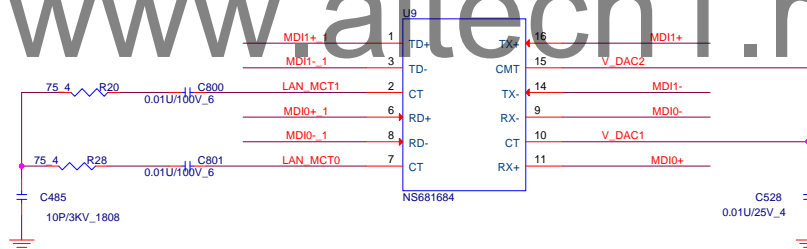
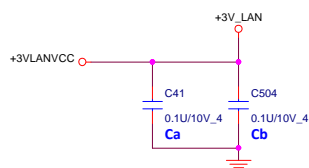




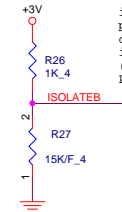
Power trace Layout 寬度> 60mil



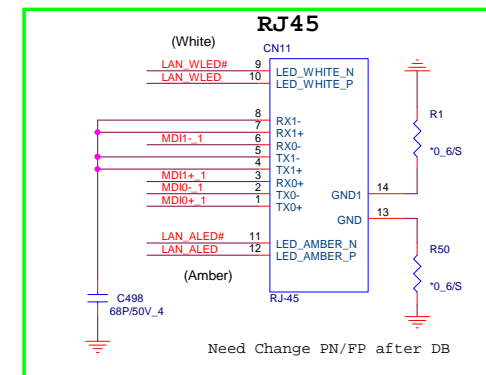
Place close PIN23 and PIN32



```
if ISOLATEB pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

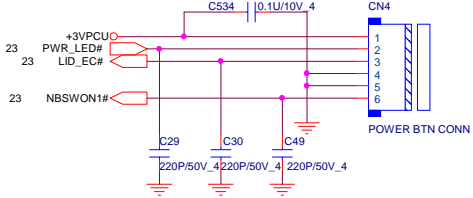


LAN conn

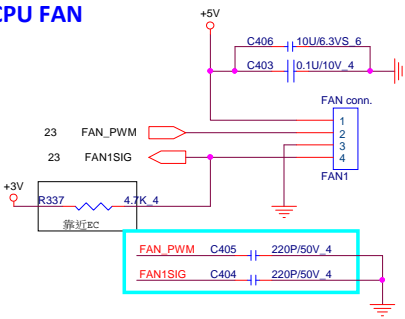


Power Button Connector

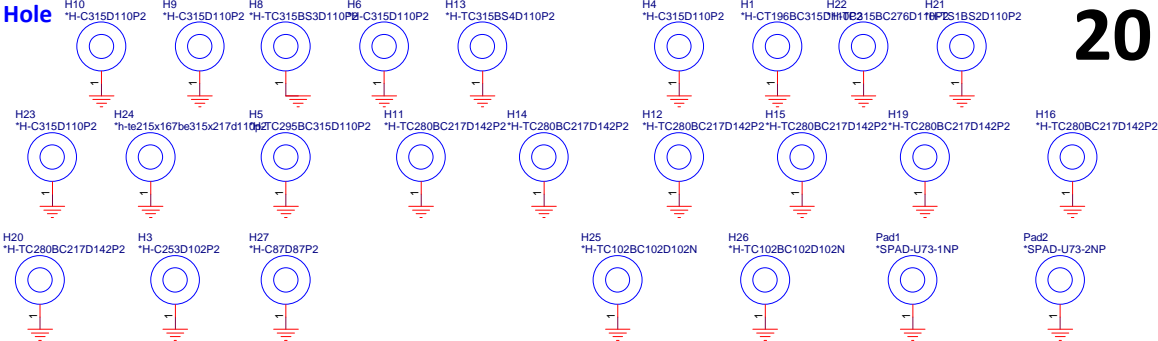
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



CPU FAN

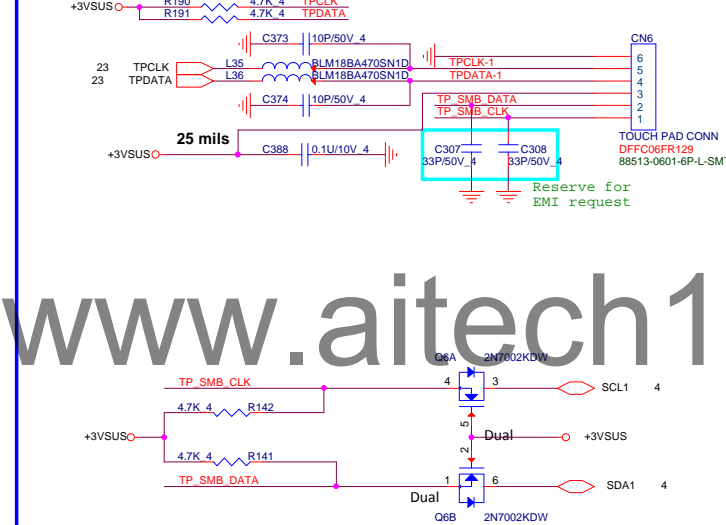
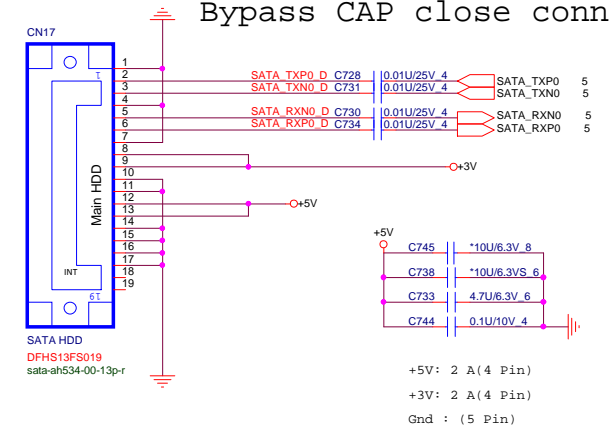


Hole



20

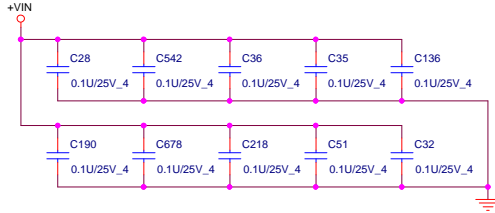
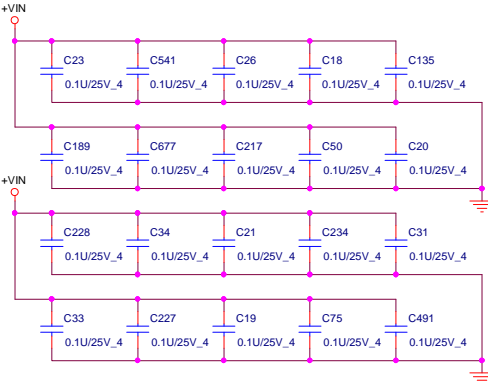
SATA HDD Connector(Cable type)



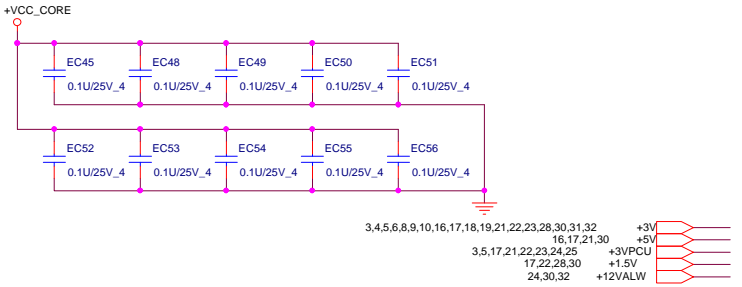
Mini PCI-E Card 2- Full size mSATA

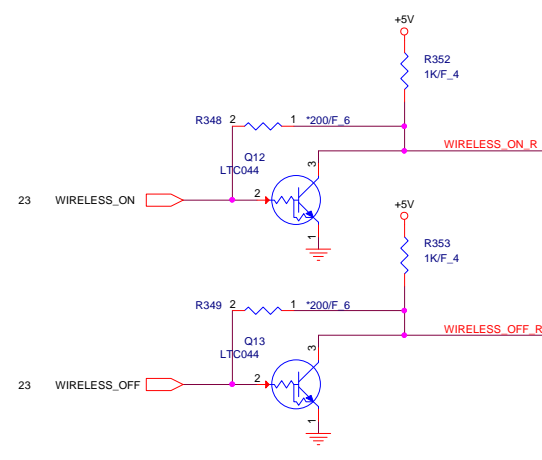
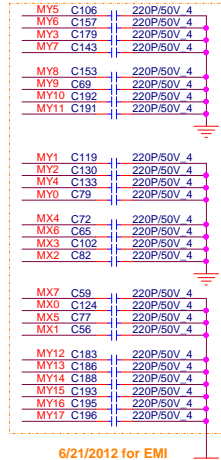
Remove

+VIN Cap

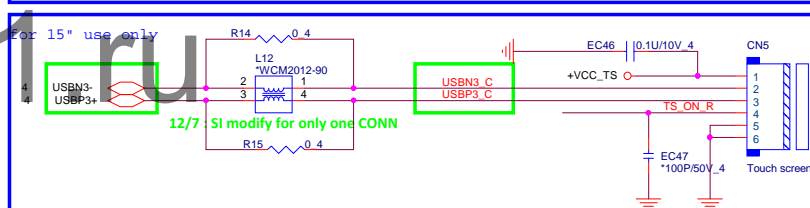


+VCC_CORE Cap

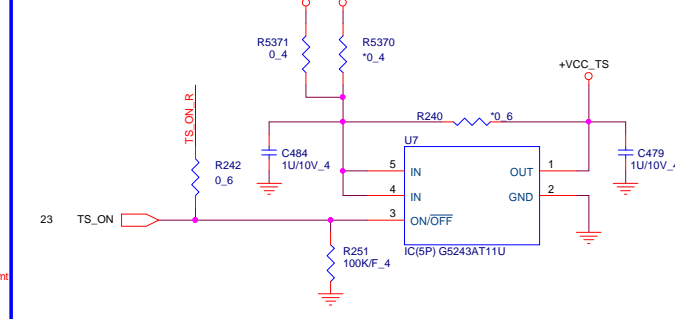




12/7 : SI Remove

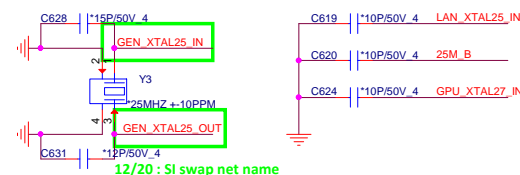


```
close to TS connector(CN5).
```

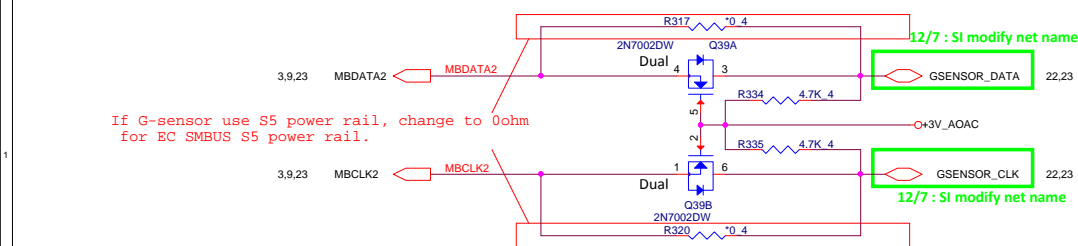


PROJECT :U73
Quanta Computer Inc.


Size Custom	Document Number USB 3.0/KB/Green CLK	Rev 1A
Date: Saturday, January 12, 2013	Sheet 21 of 32	



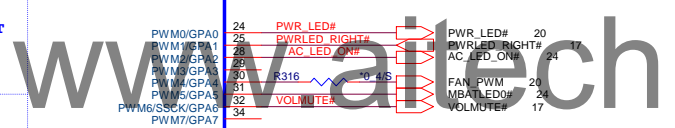
	U18 P/N
UMA	AL3NB242000
DIS	AL003357000



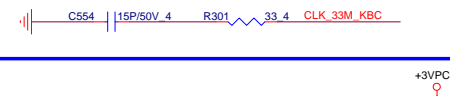
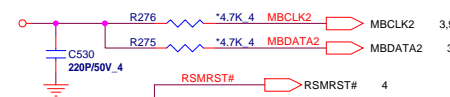
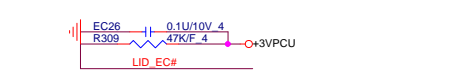
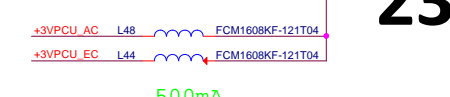
If G-sensor use S5 power rail, change to 0ohm for EC SMBUS S5 power rail.

	PROJECT :U73 Quanta Computer Inc.		
	Size Custom	Document Number MINI-PCIE/LED	Rev 1A
Date: Saturday, January 12, 2013		Sheet 22of	32

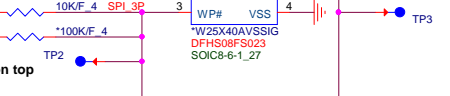
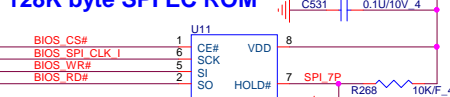
12/18 : SI modify for SERR




23



128K byte SPI EC ROM

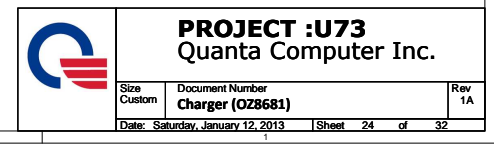


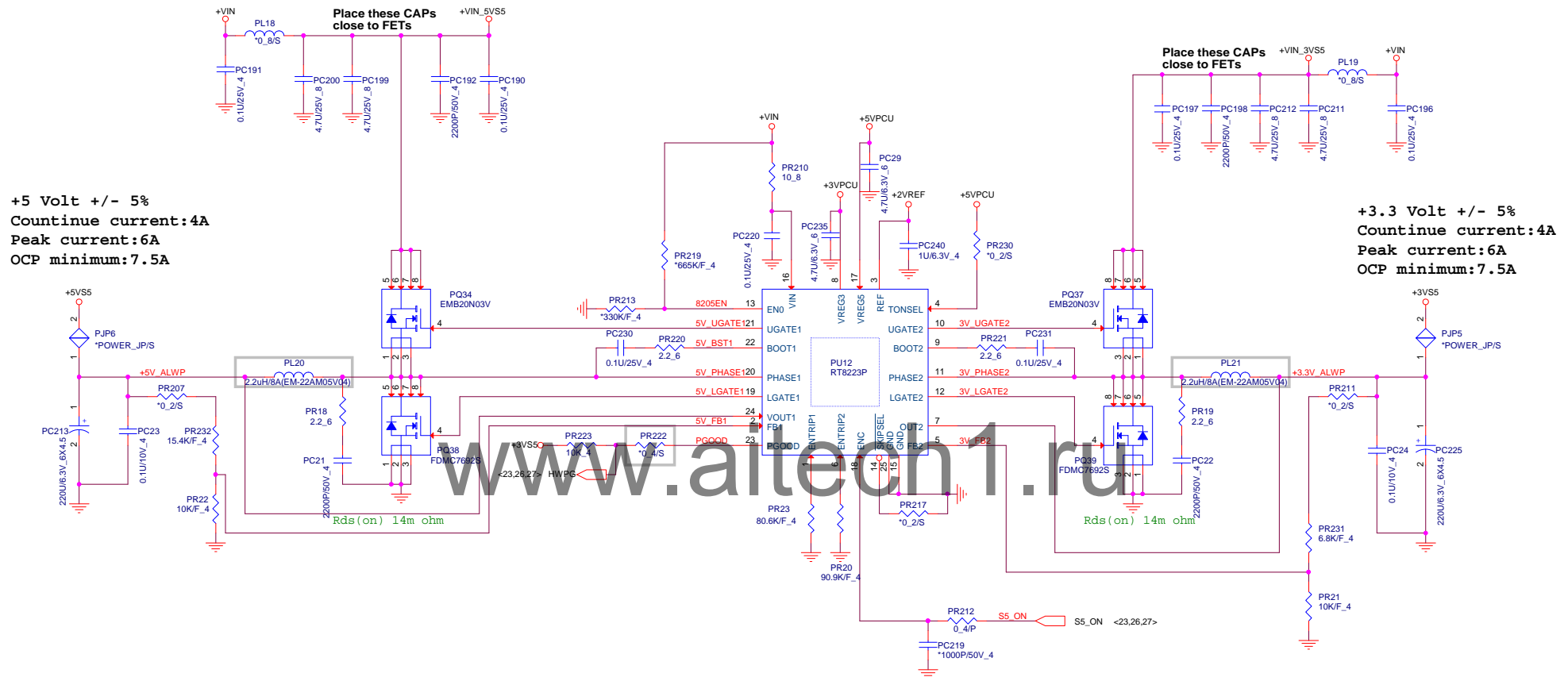
+3VPCU R319 ~~~~~ *10K/F 4 GPIO42 R318 ~~~~~ 10K/F 4

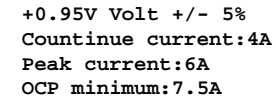
	PROJECT :U73 Quanta Computer Inc.		
	Site	Document Number	Page



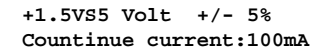
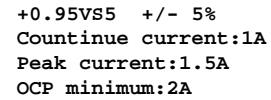
ADD VGA TEMP. FAIL function is active Hi

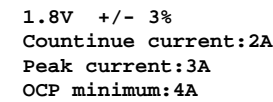
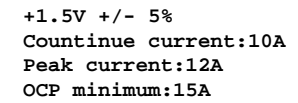




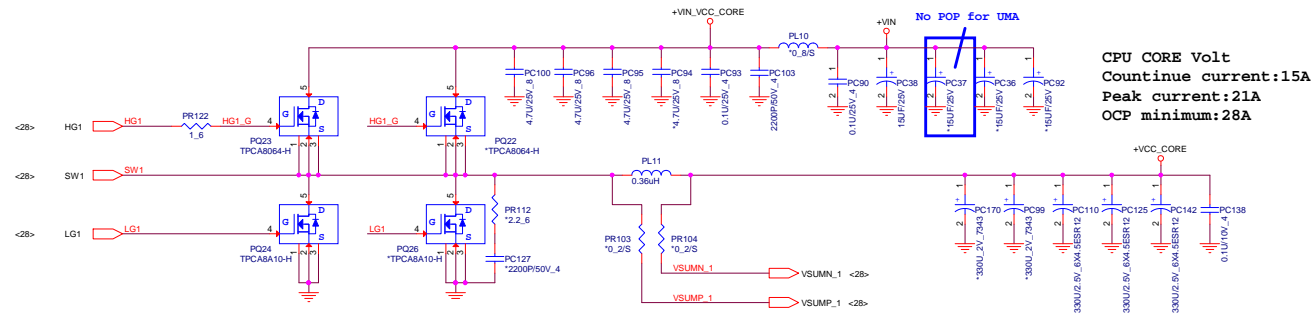


www.aitech1.ru

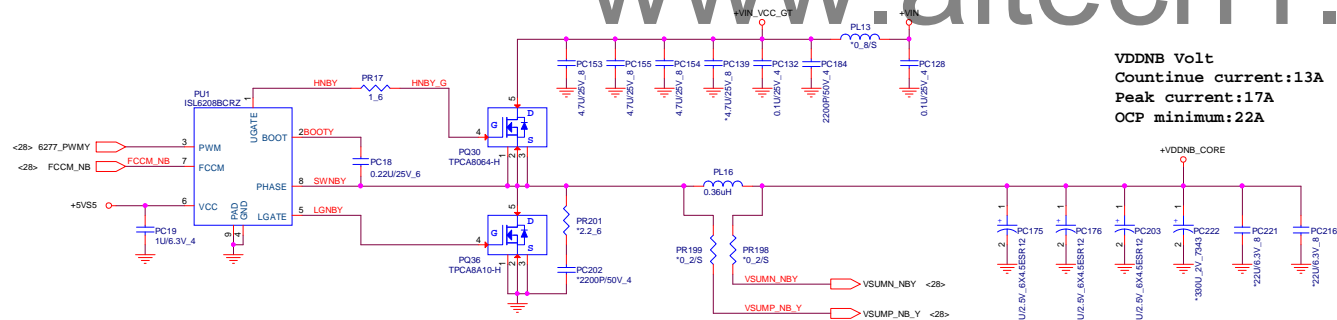






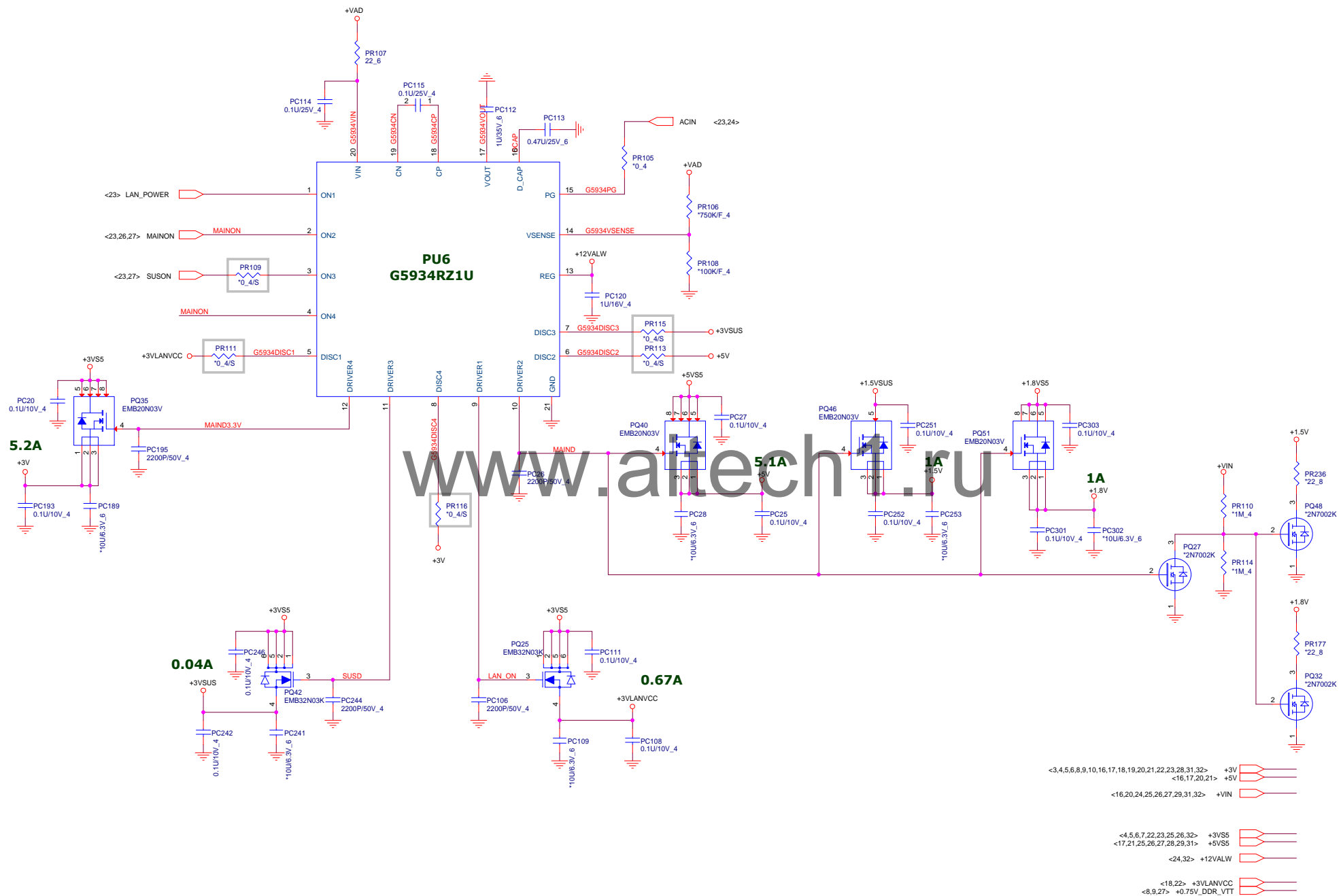


www.aitech1.ru



PROJECT :U73
Quanta Computer Inc.

Site	Document Number	Rev
Custom	ISL6208	1A
Date: Saturday, January 12, 2013 Sheet 29 of 32		



VGA Core

